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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/456,230	12/07/1999	MYLES WAKAYAMA	36159/JWE/B600	6158

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Christopher C.Winslade
McAndrewa Held & Malloy
500 W.Madison Street
Suite 3400
Chicago, IL 60661

EXAMINER
TRA, ANH QUAN

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/456,230	WAKAYAMA ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This office action is in response to the amendment filed 03/03/2003. A new ground of rejection is introduced.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 23-25, 27-29, 31, 37 and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Kozu (USP 5663687) (newly cited).

As to claim 23, Kozu discloses in figure 3 a method for providing an output signal with a characteristic frequency that is a first integer, N (M), multiple of a characteristic frequency of an input signal (signal at terminal 307), the method comprising: generating one or more oscillator signals (output of 313) with a characteristic frequency that is a second integer, M (8), multiple of the characteristic frequency of the output signal, wherein the one or more oscillator signals include a feedback signal; dividing (by circuit :8M in 310) the characteristic frequency of the feedback signal by the first integer, N (M), factor and the second integer, M (8), factor; comparing (by 311) a phase or the frequency characteristic of the feedback signal to a phase or the frequency characteristic of the input signal; and dividing (by 314) the characteristic frequency of a particular one of the one or more oscillator signals by the second integer, M (8), factor thereby, providing the output signal with the characteristic frequency that is the first integer, N, multiple, of the characteristic frequency of the input signal.

As to claim 24, figure 3 shows the step of generating a voltage (output of 311 or 312) based on the comparison between the phase or the frequency characteristic of the feedback signal to the phase or the frequency characteristic of the input signal.

As to claim 25, figure 3 shows each of the one or more oscillator signals is associated with M phases of the characteristic frequency of the output signal.

As to claim 27, figure 3 shows a phase lock loop for providing an output signal with a characteristic frequency that is a first integer, N (M), multiple of a characteristic frequency of an input signal (signal at 307), the phase lock loop comprising: a voltage controlled oscillator (313) for generating one or more oscillator signals with a characteristic frequency that is a second integer, M (8), multiple of the characteristic frequency of the output signal, wherein the one or more oscillator signals include a feedback signal; one or more divider circuits (314) for dividing the characteristic frequency of a particular one of the one or more oscillator signals by the second integer, M (8), factor thereby providing the output signal with the characteristic frequency that is the first integer, N (M), multiple of the characteristic frequency of the input signal; one or more divider circuits (:8M in 310) for dividing the characteristic frequency of the feedback signal by the first integer, N (M), factor, and the second integer, M (8), factor; and a phase detector (311) for comparing a phase or the frequency characteristic of the feedback signal to a phase or the frequency characteristic of the input signal.

As to claim 28, figure 3 shows a loop filter (312) for generating a voltage based on the comparison between the phase or the frequency characteristic of the feedback signal to the phase or the frequency characteristic of the input signal.

As to claim 29, figure 3 shows each of the one or more oscillator signals is associated with M (8) phases of the characteristic frequency of the output signal.

As to claim 31, figure 3 shows a phase lock loop for providing an output signal with a desired characteristic frequency that is an integer, N (M), multiple of a characteristic frequency of an input signal, the phase lock loop comprising: a voltage controlled oscillator (313) generating one or more oscillator signals, wherein each of the one or more signals are associated with M (8) phases of the desired characteristic frequency of the output signal; and a phase detector (311) for comparing a phase or the frequency characteristic of the input signal to a phase or frequency characteristic of a particular one of the one or more oscillator signals to the input signal.

As to claim 37, figure 3 shows a loop filter (312) for increasing or decreasing a characteristic frequency of the voltage controlled oscillator signals based on the comparison of the phase or frequency characteristic of the input signal to the phase or frequency characteristic of the particular one of the one or more reference clock signals by the detector.

As to claim 38, figure 3 shows a phase lock loop for providing an output signal with an output frequency, wherein the output frequency is an integer, N (M), multiple of an input frequency of an input signal, the phase lock loop comprising: an oscillator (313) for generating an oscillator signal with an oscillator frequency; a divider (314) for reducing the oscillator frequency of the oscillator signal by an integer, M (8), factor thereby providing an output signal with the output frequency that is the integer, N (M), multiple of the input frequency; a phase detector (311) for comparing the input signal to a feedback signal, wherein the feedback signal

has a frequency that is reduced from the oscillator frequency; and wherein the integer, N (M), is a factor for reducing the oscillator frequency to the frequency of the feedback signal.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 26 and 30-32, 35 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kozu (USP 5663687) in view of Ghoshal (USP 5068628) (previous cited).

As to claim 26, Kozu's figure 3 shows all limitations of the claim except for the step of "selecting the particular phase; and selecting the particular one of the one or more oscillator signals, wherein the M phases associated with the particular one of the one or more oscillator signals includes the particular phase". However, Ghoshal's figure 2 shows a phase locked loop circuit having a voltage control oscillator (46-56) having plurality of outputs for generating plurality of difference phase signals; a multiplexer circuit (78) for selecting particular one of output signals in order for generating a desired output signal. Therefore, it would have been obvious to one having ordinary skill in the art to use Ghoshal's oscillator circuits (46-56) and selector circuit (78) for Kozu's oscillator circuit (313) for the purpose having plurality of options to select the phase of the output signal.

Claim 30 recite an apparatus having limitation similar to claim 26. Therefore, it is rejected for the same reasons.

As to claim 32, the modified Kozu circuit shows a multiplexer (Ghoshal's 78) for selecting an output signal from the one or more oscillator signals; and a divider circuit for reducing a characteristic frequency of the output signal to the desired characteristic frequency.

As to claim 33, the modified Kozu circuit shows the multiplexer selects a particular phase, and wherein the M phases associated with the selected output signal from the one or more oscillator signals includes the particular phase.

As to claim 35, the modified Kozu circuit shows one or more divider circuits (314) for reducing the frequency of the output signal to the desired characteristic frequency, wherein the divider circuit reduces the frequency of the output signal by an integer, M (8), factor.

As to claim 36, the modified Kozu circuit shows one or more divider circuits (:8M) for reducing the characteristic frequency of the particular one of the oscillator signals by an integer, M (8), factor and an integer, N (M), factor.

5. Claim 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kozu (USP 5663687) in view of Ghoshal (USP 5068628) (previous cited) and Barrett et al. (USP 5243599) (previous cited).

The combination of Kozu and Ghoshal's references shows all limitations of the claim except for "the multiplexer selects the particular phase based on a Gray code". However, Barrett et al. shows in figure 3 a Gray code MUX with the advantage of providing faster control path than other types of decode devices. Therefore, it would have been obvious to one having ordinary skill in the art to employ the teaching of Barrett et al. in to the Ghoshal's MUX for the purpose of having faster control path.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QT
May 06, 2003

Terry D. Cunningham
Primary Examiner